IN THE CLAIMS:

1. (Amended) An arrangement [having] comprising

an electric motor (10; 10'), [having a microcontroller (12) or microprocessor, hereinafter simply called] and

a microprocessor (12), for influencing at least one motor function, having a terminal (A), wherein [which arrangement] an output on said terminal (A) of the microprocessor (12) [can be switched over] is switchable in program-controlled fashion [to] between a high level [or to] and a low level; and

further comprising a first voltage divider (20, 22) having a tapping point (18) thereof [(19) of a first voltage divider (20, 22) is] connected to [that] said terminal (A) via a resistor (17) in order to make the potential of that voltage divider tapping point (18) switchable in program-controlled fashion between at least two values by modifying that level, and by [way of that] switching said potential, to influence a parameter of the motor (10; 10').

2. (Amended) The arrangement as defined in claim 1, wherein [which]

the parameter is a current limiting value (Iref) for limiting [the] motor current (i) of the electric motor (10; 10').

3. (Amended) The arrangement as defined in claim 1 [or 2], wherein [which] said resistor (17) is of high-resistance configuration.

4. (Amended) The arrangement as defined in claim 3, wherein [which] the value of said resistor (17) is not less than 50 kilohm [or more].

5.(Amended) The arrangement as defined in [one or more of] claim[s] 1 [through 4], wherein [which] said output [(A)] of the microprocessor (12) [can be switched over] is switchable in program-controlled fashion to a third, high-resistance, state [(FIG. 4)].

6.(Amended) The arrangement as defined in [one or more of the foregoing claims] claim 1, wherein said first voltage divider has branches and [which]

there is provided, parallel to one branch (22) of the first voltage divider (20, 22), a second voltage divider (160) having a tapping point (163), the potential at the latter tapping point (163) influencing the parameter of the motor (10; 10').

7.(Amended) The arrangement as defined in claim 6, wherein [which] the second voltage divider (160) has a higher resistance as compared to the resistance value of the branch (22) of the first voltage divider (20, 22) to which it is connected in parallel.

8.(Amended) The arrangement as defined in claim 6 [or 7], wherein [which] the voltage division ratio of the second voltage divider (60) is designed so that, when the potential at its tapping point (163) is used as a comparison potential, the result is a low[er] value for that comparison potential.

9.(Amended) The arrangement as defined in [one of more of] claim[s] 6 [through 8, in which] wherein

the potential at the tapping point (163) of the second voltage divider (160) defines a current limiting value (Iref) for limiting the motor current (i) of the electric motor (10; 10').

10.(Amended) The arrangement as defined in claim 2 [or 9], [having] comprising

a nonvolatile memory element (14) [which serves] serving to store at least one time value (Ts) after whose expiration a switchover of said output (A) of the microprocessor (12) is accomplished in program-controlled fashion.

Please add a new dependent claim:

41. The arrangement as defined in claim 9, comprising

a nonvolatile memory element (14) serving to store at least one time value (Ts) after whose expiration a switchover of said output (A) of the microprocessor (12) is accomplished in program-controlled fashion.

11. (Amended) A method [for] of controlling the startup of an electric motor [with which a microcontroller or microprocessor, hereinafter called] comprising

an associated control circuit including a microprocessor (12), a nonvolatile memory [element] (14), a data bus (13, 15) interconnecting said microprocessor and memory element, and an arrangement, coupled to an output of said microprocessor, for limiting the motor current (i), [are associated for control purposes, the method having] comprising the following steps:

storing, in the nonvolatile memory, [an acceleration] a startup time (Ts) [is stored] via the data bus (13, 15) [in the nonvolatile memory element (14)];

switching on [after] the motor [is switched on, that] and thereafter monitoring the startup time (Ts) of said motor [acceleration time (TS) is monitored];

during [that acceleration] said startup time (Ts), setting, under control of a program running in said microprocessor, a [the] current limiting value (Iref), of the arrangement for limiting the motor current (i), [is set in program-controlled fashion] to a first value (Iref = 1);

[when it is ascertained that the] ascertaining expiration of said startup [acceleration] time (Ts) [has expired,] and thereafter, in a program-controlled manner, setting the current limiting value (Iref) [is switched over in program-controlled fashion] to a second value (Iref = TST) that is different from the first value.

12. (Amended) The method as defined in claim 11, wherein [which] the second current limiting value is less than the first current limiting value.

13. (Amended) The method as defined in claim 11 [or 12], further comprising [in which, after]

upon expiration of the acceleration time (Ts) [has expired], [a determination is made as to] determining whether motor current limiting [is] has been effective during a time span that exceeds a predefined time span;

and if such [is the case] current limiting has been effective during said time span, changing the current limiting value (Iref) [is switched over] in program-controlled fashion to a third value (Iref = 0).

14. (Amended) An arrangement for carrying out [the method as defined in one or more of claims 11 through 13,] program-controlled adjustment of limitation of current passing through windings of a motor controlled by an associated microprocessor (12) wherein [which]

the microprocessor (12), for program-controlled switchover of [the] a current limiting value (Iref), comprises [has] at least one terminal whose output signal [(A) that can be switched over] is switchable at least between a high and a low signal level and thereby influences the current limiting value (Iref);

and [that] wherein said output signal level is modifiable [can be modified] in program-controlled fashion during [acceleration] startup of the motor (10; 10').

15. (Amended) The arrangement as defined in claim 14, wherein [which] the at least one output (A) [can be switched over] is switchable to a high-resistance state called the tristate state.

16. (Amended) The arrangement as defined in claim 14 [or 15], wherein [which] the output (A) serving to switch over the current limiting value is connected via a resistor (17) to [the] a tapping point (18) of a first voltage divider (20, 22), the potential at that tapping point (18) serving for comparison with a voltage (u) at a measurement resistor (36) through which the motor current (i) flows;

and wherein the motor current (i) [being] is interrupted when that voltage (u) reaches a predefined ratio with respect to that potential.

17. (Amended) The arrangement as defined in claim 16, wherein [which] there is provided, parallel to one branch (22) of the first voltage divider (20, 22), a second voltage divider (160) having a tapping point (163), the potential at the latter tapping point (163) serving for comparison with a voltage (u) at a measurement resistor (36) through which the motor current (i) flows;

and wherein the motor current (i) [being] is interrupted when that voltage (u) reaches a predefined ratio with respect to that potential at the latter tapping point (163).

18. (Amended) The arrangement as defined in claim 17, [in which] further comprising a comparator (28) is [provided for] serving to make a comparison with a voltage (u) at a measurement resistor (36) through which the motor current (i) flows.

19. (Amended) The arrangement as defined in claim 17 [or 18], wherein [which] the second voltage divider (160) has a higher resistance as compared to the branch (22) of the first voltage divider (20, 22) to which it is connected in parallel.

20. (Amended) The arrangement as defined in [one or more of] claim[s] 17 [through 19], wherein [which the] a voltage division ratio of the second voltage divider (60) is [designed] so chosen that, when the potential at its tapping point (163) is used as a comparison potential, the result is a low[er] value for that comparison potential.

21. (Amended) The arrangement as defined in [one or more of] claim[s] 18 [16 through 20], wherein [which] the voltage (u) at the measurement resistor (36) is filtered [through] by a low-pass [element] filter (38, 42) before comparison with the aforesaid comparison potential.

22. (Amended) The arrangement as defined in claim 21, [in which] wherein the low-pass element is configured as a first-order low-pass [element] filter (38, 42).

23.(Amended) An arrangement [having] comprising

an electric motor (10; 10'), [in particular] adapted for driving a fan (73), [having a microcontroller (12) or microprocessor, hereinafter simply called]

a microprocessor (12), for influencing at least one motor function, there being associated with that microprocessor (12) a volatile memory element (330) and a nonvolatile memory element (14), [which] said memory elements being configured for storing at least one object as a definition for that motor function;

[further having] an interface (13a), associated with the electric motor, for a data line (13; 210, 226) for transferring that at least one object [to and/or from] between said microprocessor and a memory element (14, 330),

and [having]

a stored directory (280), associated with the microprocessor (12), which contains, for objects that are transferable via the data line (13, 210, 226), predefined parameters (286, 288, 290) for the transfer of those objects.

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24.(Amended) The arrangement as defined in claim 23, [in which] wherein

the stored directory (280) contains data (286) as to the length of transferable objects.

25.(Amended) The arrangement as defined in claim 23 [or 24, in which] wherein

the stored directory (280) contains data (288) as to whether the relevant object is intended for storage in the nonvolatile memory element (14) or in a volatile memory element (330).

26. (Amended) The arrangement as defined in [one or more of] claim[s] 23 [through 25], wherein [which]

the stored directory (280) contains data (290) as to the address of the object in a memory element (14, 330).

27. (Amended) The arrangement as defined in [one or more of] claim[s] 23 [through 26, in which] wherein

the stored directory (280) is stored in a nonvolatile and [, in particular,] permanent fashion in a memory (336) associated with the microprocessor (12).

28. (Amended) The arrangement as defined in claim 27, wherein [which]

the stored directory (280) is a hardware component of the microprocessor (12).

29. (Amended) The arrangement as defined in [one or more of] claim[s] 23 [through 28], wherein [which]

the microprocessor (12) is connected to the interface (13a) for the data line (13);

and the transfer of objects from and/or to the nonvolatile memory element (14) is accomplished via the microprocessor (12).

30. (Amended) The arrangement as defined in [one or more of] claim[s] 23 [through 29], wherein [which] the data line is [configured as] a serial data bus (13, 210, 226).

31. (Amended) The arrangement as defined in [one or more of] claim[s] 23 [through 30, in which] wherein at least one buffer memory (332) for data traffic with a data line (13; 15) is provided in the volatile memory (330) associated with the microprocessor (12).

32. (Amended) The arrangement as defined in [one or more of] claim[s] 23 [through 31, in which] wherein the nonvolatile memory element (14) is connected [via a line (CS)] to the microprocessor (12) via a line (CS) which, controlled by the microprocessor (12), influences a write protection of the nonvolatile memory element (14).

33. (Amended) The arrangement [as defined in one or more of] according to claim[s] 23 [through 32, in which] wherein the microprocessor (12) comprises [has]

a predefined memory element (332) for storing an address [(FIG. 17: 242; FIG. 18: 254)] conveyed via the data line (13), an arrangement (14, 330) for storing an address (324) of the arrangement to be addressed, and a comparator[ison arrangement] for comparing those two addresses.

34. (Amended) The arrangement [as defined in one or more of] according to claim[s] 23 [through 33, in which] wherein a memory element (332), for storing a variable [(FIGS. 18, 19: 246; FIG. 18: 254)] that characterizes an object to be transferred, is associated with the microprocessor (12); and by [way of] using that variable, at least one characteristic (286, 288, 290) of that object can be [taken] retrieved, for processing thereof, from a directory (280) stored in the arrangement.

35. (Amended) The arrangement as defined in claim 34, wherein [which] the characteristic is the length (286) of that object.

36. (Amended) The arrangement as defined in claim 34 [or 35, in which] wherein the characteristic is the hardware address (288, 290) of that object.

Please cancel claims 37-40, without prejudice.